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MOTOROLA
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ANE 001/D
Application Note

32-BIT COMPUTER DESIGN USING 68020/68881/68851

INTRODUCTION

This application note describes the design of a small, general-purpose, high-performance computer based on Motorola's 32-bit MC68020 microprocessor. A MC68881 FPCP (Floating-Point CoProcessor) provides high-speed, high-accuracy floating-point mathematics and executes as a tightly-coupled coprocessor to the MPU. A MC68851 PMMU (Paged Memory Management Unit), also a co-processor, provides resource protection and logical-to-physical address translation required by multi-tasking operating systems. It also helps the MC68020 support virtual memory and virtual machine techniques.

A MC68681 DUART (Dual-channel Universal Asynchronous Receiver Transmitter) and associated circuitry provide two serial RS232 ports for connection to terminals or for computer-computer links. A MC68230 PI/T (Parallel Interface/Timer) is used for a Centronics-type parallel printer port and a hardware timer.

One megabyte of read/write memory for program code and data is implemented with 32 MCM6256 256k bit dynamic RAMs. A random logic DRAM controller is described. There are 64k bytes of read-only memory suitable for initialization code and debug monitor firmware using eight 64k bit EROMs.

DESCRIPTION OF OPERATION

The MPU and FPCP appear to the rest of the system as a single CPU (Fig. 1*). The PMMU is placed between the MPU/FPCP pair and the memory and peripherals, thus the MPU/FPCP reside on the logical address bus LA[0:31] and only the MPU and PMMU access it. The FPCP is a non-DMA type coprocessor and acts as a slave to the microprocessor. Addresses generated by the MC68020 are translated by the PMMU which presents the physical address PA[0:31] (buffered physical address lines denoted by BA[0:31]) to the memory and peripherals. CPU Address Space decoder logic (U110, U111 and U112A) monitors the MPU function codes (FC[0:2]) and portions of the logical address bus (LA[13:17]) to determine CPU address space functions. It generates a chip-select for the FPCP (ECOP1*) and the interrupt acknowledge signal IACK. The M68000 family coprocessor interface directly supports up to eight coprocessors: the FPCP is assigned to be coprocessor #1; the PMMU is coprocessor #0 by default (decoded internally by the PMMU).

The MPU/FPCP data bus is buffered from the rest of the system by four 74LS245 octal transceivers (U103-U106). Their enable signal G* is derived from the FPCP chip-select and the MC68020 Data Bus ENable (DBEN*).

PHYSICAL ADDRESS DECODER

Addresses produced by a physical bus master (PMMU or DMA-type peripheral) are decoded to generate the enable signal for each memory or peripheral device. The use of physical (rather than logical) addresses prevents access to peripherals by unauthorized software tasks as only the operating system is aware of their physical addresses. Also the non-systems programmer dealing with logical address information need not be concerned as to the actual whereabouts of main memory.

High-order physical address lines BA[20:22] are used to allocate equal-sized portions of the address space between the physical bus memory and peripherals. A 74F138 3-to-8 line decoder (U213) generates enable signals for up to eight devices (Fig 2B). Each is conditioned by the physical address strobe (PAS*) so that no device is enabled during CPU space accesses or during address setup times. Signals EROM*, ERAML* and ERAMH* are assigned to 32-bit program and read/write memories, EDUART*, EPIT* and E8A* for 8-bit devices, and E16A* and E16B* for 16-bit devices. For certain devices such as program ROM or simple peripherals these enable signals may be used directly as chip-selects. For example, the program code EROMs (U400-U407) are chip-selected by EROM* causing them to drive all four bytes of the data bus regardless of whether the MC68020 is performing a byte, word or long word read from this memory.

To fully support the MC68020's dynamic bus sizing capability the RAM circuitry has separate chip-select signals for each parallel byte occupied by the device on the data bus. These are generated by conditioning the enable signals with three signal groups:

1) the least significant two address lines (BA[00:01]) to determine the alignment of the operand being transferred with respect to the nearest long word boundary;
2) SIZ[0:1], to indicate the maximum number of bytes which could be transferred; and

*See foldout page at the back of this application note.

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3) the port size (P8*, P16* and P32*) of the device. An 82S153A FPLA (U215) monitors these signals to generate four enable signals (E0007*, E0815*, E1623* and E2431*) used for the parallel byte chip-selects. The FPLA is programmed to reflect the truth table shown in table 5-6 of the MC68020 user's manual.

PROGRAM ROM

Fig. 4 shows a 64k byte program ROM (organized as 16k long words) implemented using two banks of four MCM68764 EROM's (U400-U407) or similar devices. Jumper block J400 allows either the 24- or 28-pin devices to be populated. A 74LS174 hex D-type flip-flop (U408) uses the ROM chip-select signal (EROM*) to generate the DSACK[0:1]. Jumper block J401 allows the DSACK timing to be varied to suit ROM's with access times of 250, 300 and 350 ns.

READ/WRITE MEMORY

Many MC68020-based computer systems will have read/write memory of one megabyte or more in size. Implementing such memories using 256k bit dynamic RAM's represents a good compromise between performance, cost and packing density. Figure 3 shows a one megabyte memory consisting of 32 MCM6256-12 2546k bit 120ns DRAM's. Allowing for address translation times via the MC68851 PMMU the MPU can perform five-cycle read and write operates on the memory (i.e. with two wait cycles). For higher performance, but at increased cost, 100ns DRAMs could be used to construct a memory with a four-cycle access time.

To fully support the MC68020's flexible bus operation the memory is organized as four separate parallel byte-wide blocks. Each block resides on one of the four bytes of the MC68020's 32-bit data bus. Four memory address strobes (CASL[0:3]) allow the microprocessor to independently access any byte or bytes at a given 32-bit address.

Provision is made for a second one-megabyte memory. It would be identical to that shown in Figure 3 except its strobes (CASH[0:3]) are conditioned with ERAMH* instead of ERAML*.

DYNAMIC RAM CONTROLLER

Dynamic random-access memories require both address multiplexing and refreshing. In Figure 2B an 18-bit address (BA[02:19]) from the CPU is formed into two (row and column) 9-bit memory addresses (MA[0:8]) using three 74F157 quad 2-to-1 line multiplexers (U210-U212). These addresses, like other signals driving the memory array have small series resistors placed close to the output devices to help minimize transmission line effects.

A DRAM control sequencer (Figure 2A) is responsible for generating the row-to-column changeover signal (ADS), the row and column address strobes (RAS* and CAS*) and the DRAM data transfer acknowledge and port size signals (DSACK[0:1]*). Whenever the CPU accesses the memory a 'RAS before CAS' sequence is used (Figure 2C). In this mode ERAML* or ERAMH* allows a logic "0" to propagate through successive Q_n* outputs of a 74F175 quad D-type flip-flop (U201) asserting the DRAM control signals

on successive positive-going edges of the master system clock (CLK33).

Approximately every 15 us the DRAM's must be refreshed. One half of a MC3456 dual timer (U206A) produces a refresh clock (REFCLK) whose negative-going clock edge initiates a 'CAS before RAS' sequence (with no active DSACK signal). Applying CAS before RAS causes all DRAM's to perform a refresh of the next row of memory cells as determined by an on-chip row address register. The Q7 output of a 74LS165 parallel-load shift register (U209) sets the sequencer into 'refresh mode'. The 74F157 quad 2-to-1 line multiplexer U200 switches from the normally-selected 'A' inputs to the 'B' inputs thereby changing the order in which the DRAM control signals are generated (Figure 2C).

Since there is an asynchronous relationship between refreshes and CPU bus cycle accesses to memory, an 'access collision' can occur. To overcome this the cross-coupled NAND gates U207A and U207B prevent the refresh mechanism from operating until the CPU has completed its current bus cycle access to memory. However, if the CPU attempts to begin a bus cycle access to memory while the DRAM's are being refreshed the refresh mechanism is allowed to complete it's 'CAS before RAS' sequence (with DSACK inhibited) before the CPU 'RAS before CAS' cycle can start. In this case the access appears normal to the CPU except that additional wait states are inserted. This refresh technique is faster than bus arbitration methods but requires more hardware logic to implement.

SERIAL COMMUNICATIONS

The DUART (U500) provides two serial communications ports. Typically they are used for local terminals and links to host computers. MC1488 drivers (U505-U507) and MC1489A receivers (U504) provide the TTL-RS232 voltage level translation between the DUART and the ports (Figure 5). Jumper blocks J500 and J501 allow each port to be configured either as Data Set or Data Terminal.

74LS74A D-type flip-flops (U501 and U502) and gates U503A and U503B ensure the minimum chip-select negated period for the MC68681 is achieved. This time can only be violated by a 16 MHz MC68020 performing repeated accesses to DUART registers from 'tight loop' software executing from the on-chip instruction cache. In all other cases this logic is redundant and may be omitted where this situation cannot occur and EDUART* can be used directly as the DUART chip-select.

PARALLEL PRINTER PORT

Figure 5 shows a Centronics-type parallel printer port implemented using a MC68230 PI/T (U508). Buffering of outputs is provided by a 74LS244 octal driver (U509) and gates U503C and U503D. To ensure proper operation during internal register accesses, the PI/T chip-select EPIT* is conditioned by the MC68020 data strobe DS*.

The PI/T also provides a general-purpose 24-bit timer, which may for example be used by an operating system scheduler to generate periodic hardware interrupts.
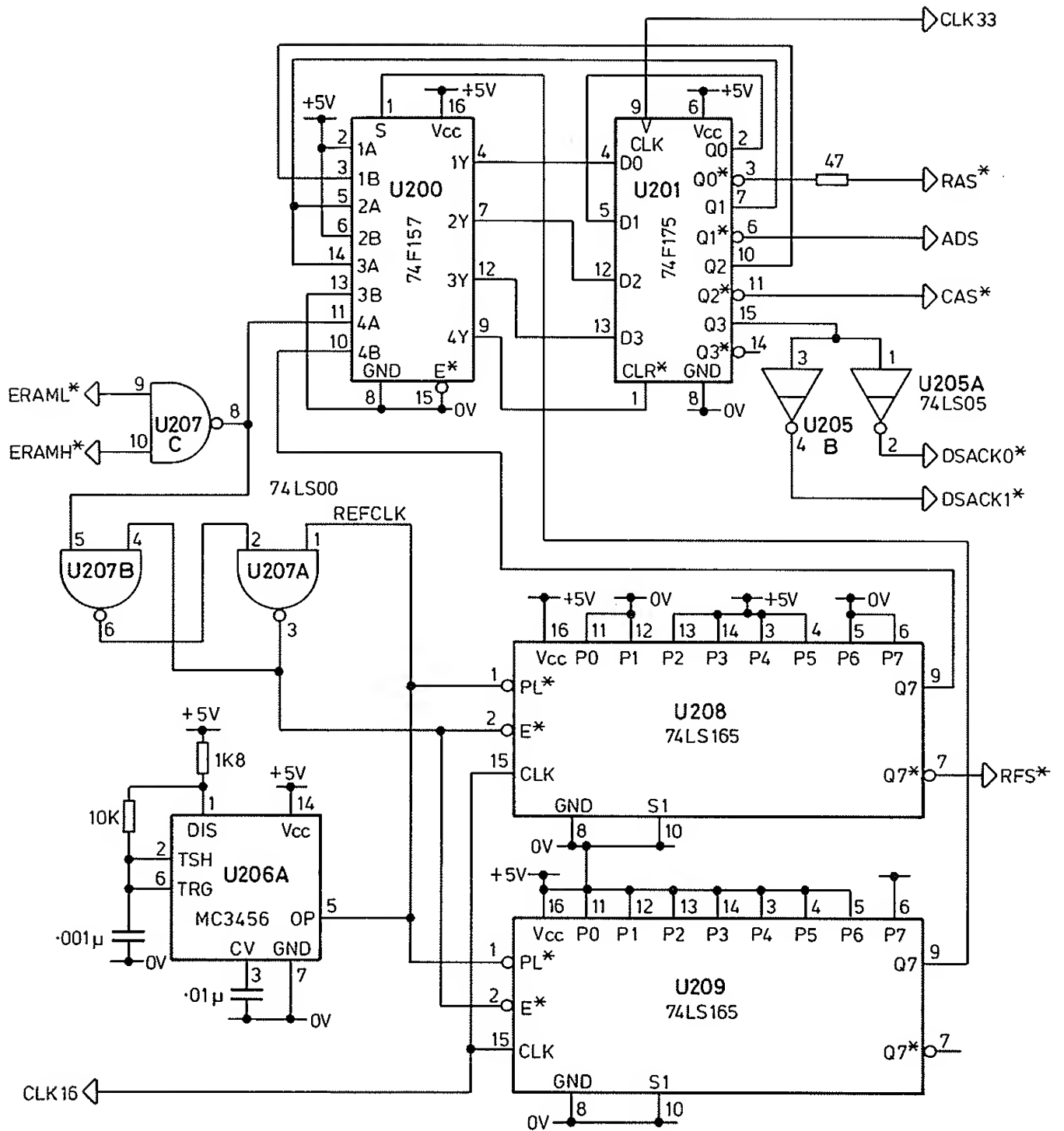
FIGURE 2A – Dynamic RAM Refresh Controller

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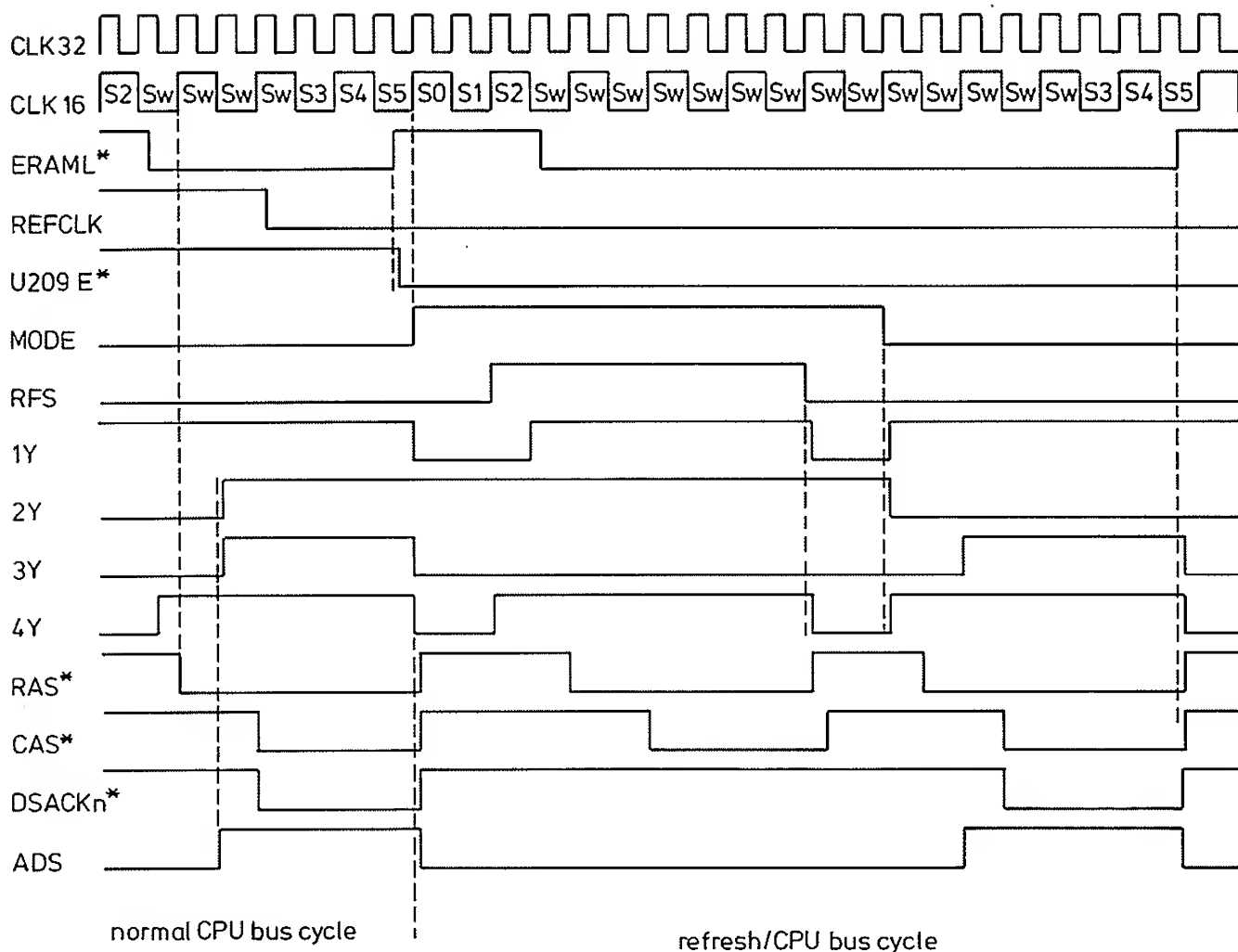FIGURE 2B – Physical Address Decoder & Dynamic RAM Control

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FIGURE 2C – DRAM Control Sequencer Timings

OTHER CIRCUIT ELEMENTS

See Figure 6. The master system clock source (CLK33) is a TTL compatible monolithic crystal oscillator (U600) with a frequency of 33.33 MHz. Some vendor's oscillators of this type do not meet the undershoot voltage requirements of MOS/TTL devices and some clamping may be required. Other clocks required in the system are derived from CLK33 using a 74LS93 4-bit binary counter (U601).

The MC68020 directly supports seven priority levels of hardware interrupt. All are supported here but only four are currently assigned: two for the PI/T (the parallel interface and the timer), the DUART and the manual abort (MA). MA is generated from the abort switch S2 via the debounce gates U604C and U604D. By using the MC68020's non-maskable level #7 interrupt it provides a means of manually aborting any executing program and returning in a controlled manner to the ROM-based firmware. All other interrupt sources may be assigned to levels #1 to #6 by use of jumper block J600 and J601. The interrupts are priority encoded via U603 which presents the 3-bit encoded interrupt level IPL[0:2] to the MPU. A 74LS138 3-to-8 line

demultiplexor (U602) generates the individual $IACK_n$ signals required by the interrupting periphals as part of the interrupt acknowledgement sequence. As the MA logic cannot generate its own interrupt vector number during IACK, AVEC is asserted instead of DSACK to indicate the use of an autovector.

A system watchdog timer (WDT) monitors bus cycle activity and informs the MPU or other bus master that an access to a non-decoded address space location was made, or that a slave device has failed to perform the hardware handshaking for the current bus cycle. A 74LS174 hex D-type flip-flop (U605) triggered by LAS* or PAS* asserts the bus error (BERR*) signal if the bus cycle does not terminate within a reasonable time. LAS* is included to detect the non-existence of hard-ware related to CPU Address Space functions such as coprocessor and breakpoint acknowledgement accesses (the PMMU does not generate PAS* in such cases). The WDT timeout period is set longer than the bus cycle time for the slowest slave device in the system.

An MPU halt state indicator (U606 and CR1), power-on reset (U206B, U604 and U606) and manual reset (U604 and switch S1) are shown in Figure 6.
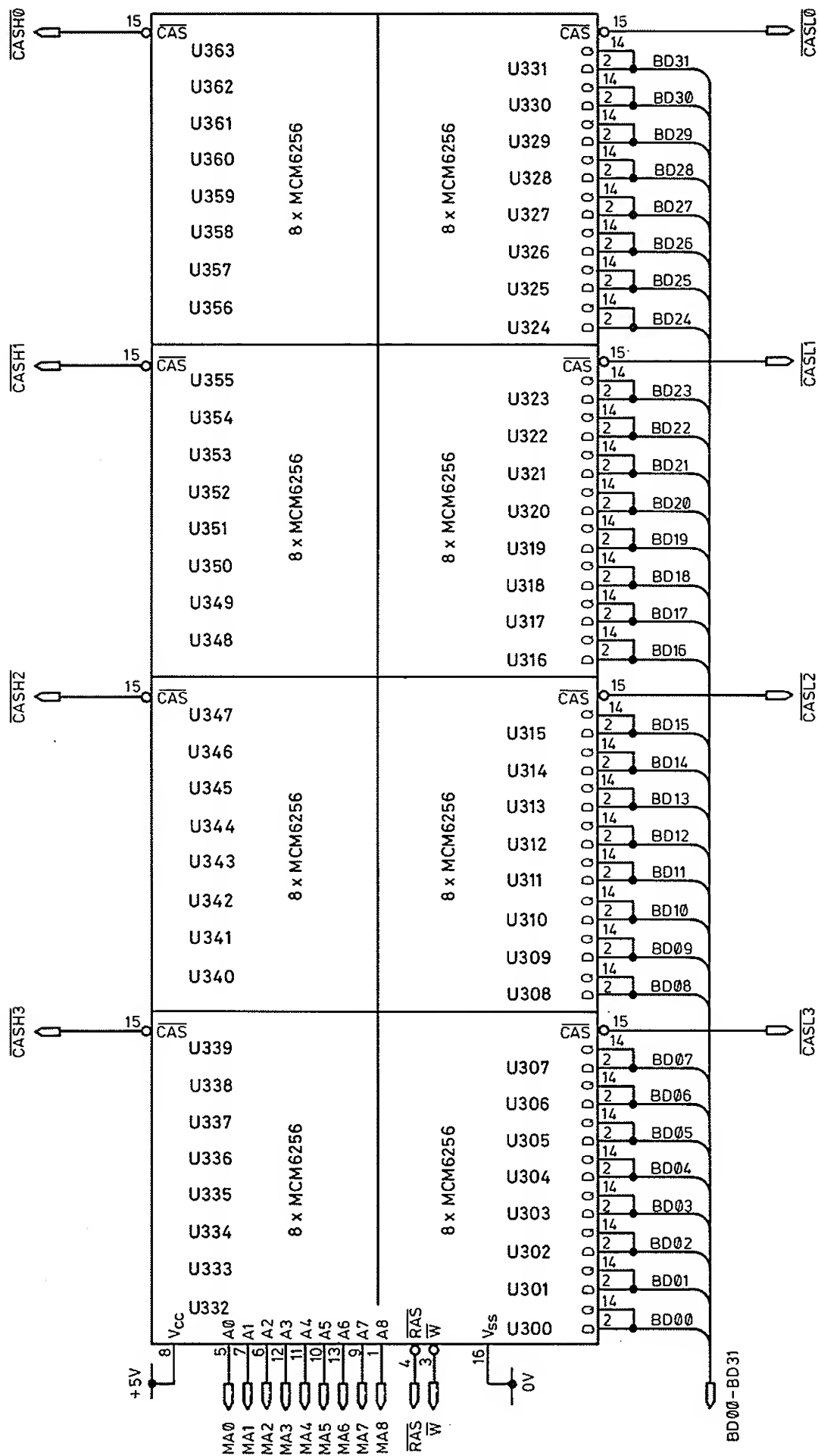
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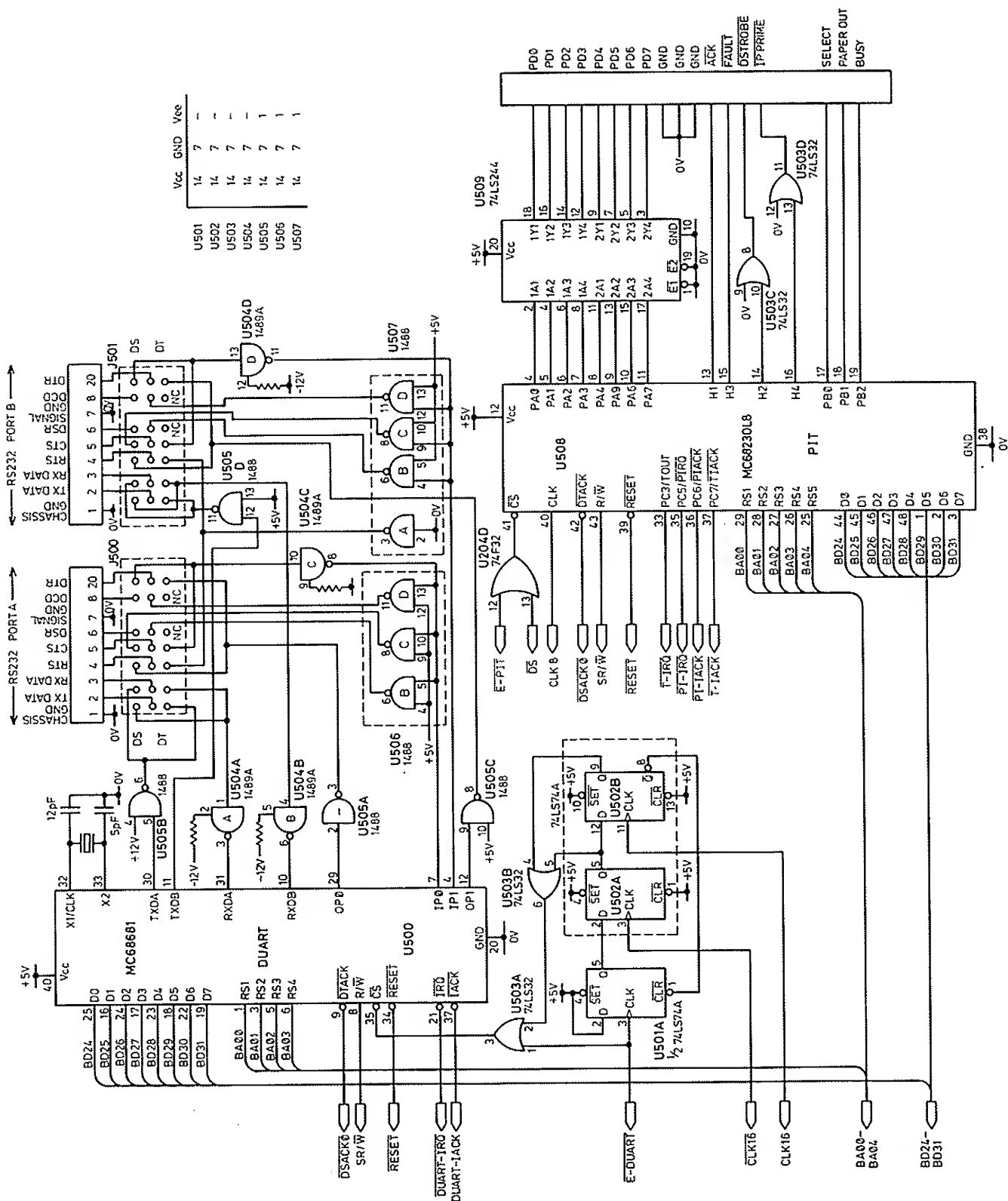FIGURE 3 – 68020/FPCP/PMMU Application – 2M Byte Dynamic RAM

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FIGURE 4 – 68020/FPCP/PMMU Application 64k Byte ROM

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FIGURE 5 – Dual Serial Ports/Parallel Printer Port

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FIGURE 6 - Miscellaneous

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